wherein the power control means supply power to said memory integrated circuit, said power being supplied to the memory integrated circuit at a first variable voltage level during periods of no data access activity and at a second variable voltage level during periods of data access activity, [a] the variable voltage supplied at said first variable voltage level being less than [a] the variable voltage supplied at said second variable voltage level,

wherein the power supplied at the first level is [greater than or equal to a power necessary] sufficient to preserve information stored in the integrated memory circuit and the power supplied at the second level is [greater than or equal to the power required] sufficient to read and write information in the integrated memory circuit.

23. (Four Times Amended) A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source supplying a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory integrated circuit, said variable voltage being less than or equal to said substantially constant voltage supplied by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for controlling said power control means;

wherein the power control means supply power to said memory integrated circuit, said power being supplied to the memory integrated circuit at a first variable voltage level during periods of no data access activity and at a second variable voltage level during periods of data access activity, [a] the variable voltage supplied at said

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first variable voltage level being less than [a] the variable voltage supplied at said second variable voltage level,

wherein the power supplied at the first level is [greater than or equal to a power necessary] sufficient to preserve information stored in the integrated memory circuit and the power supplied at the second level is [greater than or equal to the power required] sufficient to read and write information in the integrated memory circuit.

## REMARKS

Claims 1-23 are pending in the above-referenced application. In the Office Action of April 25, 1997, the Examiner rejected Claims 1-20 and 23 under 35 U.S.C. § 112, as containing subject matter not enabled by the Specification.

Claims 1 and 23 are amended herewith to only clarify the scope of the claims. The amendment is not made to distinguish any prior art nor to limit the scope of Claims 1 and 23 in any fashion. The Examiner stated in his Office Action of April 25, 1997 that the last six lines of Claims 1 and 23 recite different subject matter than the subject matter disclosed in the Specification. In accordance with the Examiner's suggestion in his informal telephone communication with Applicant's attorney on April 16, 1997, Applicant respectfully submits these changes to bring the Claims into correspondence with the Specification and requests withdrawal of the Examiner's rejection.

The Examiner further rejected Claims 1-23 under 35 U.S.C. § 102(a), as being anticipated by Nakatani et al. (US Pat. No. 5,297,098). In the Office Action of April 25, 1997, the Examiner stated "[a]s per claims 1 and 23, Nakatani discloses supplying a variable voltage to said memory integrated circuit (column 3, lines 13-18 and figure 1), generating address and control signals for said memory integrated circuit (figures 5-7 and column 6, lines

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